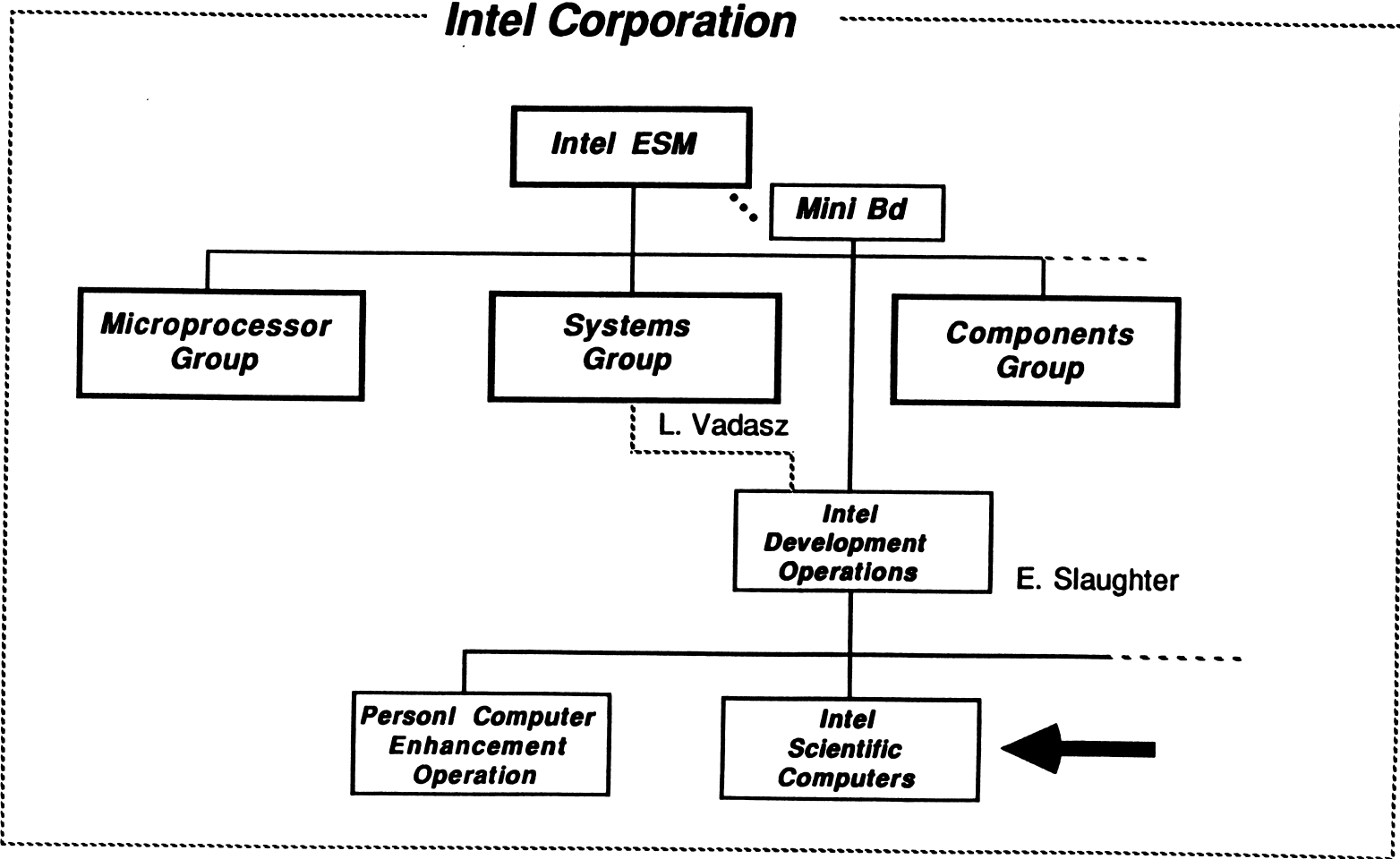


Intel Scientific Computers

- **Organization**
 - ***a business unit of Intel Development Operations***
- **iDO Charter**
 - ***to develop strategic new businesses for Intel***
- **iSC Charter**
 - ***apply Intel's VLSI technology to large-scale scientific computing***
- **Location**
 - ***Beaverton, Oregon***

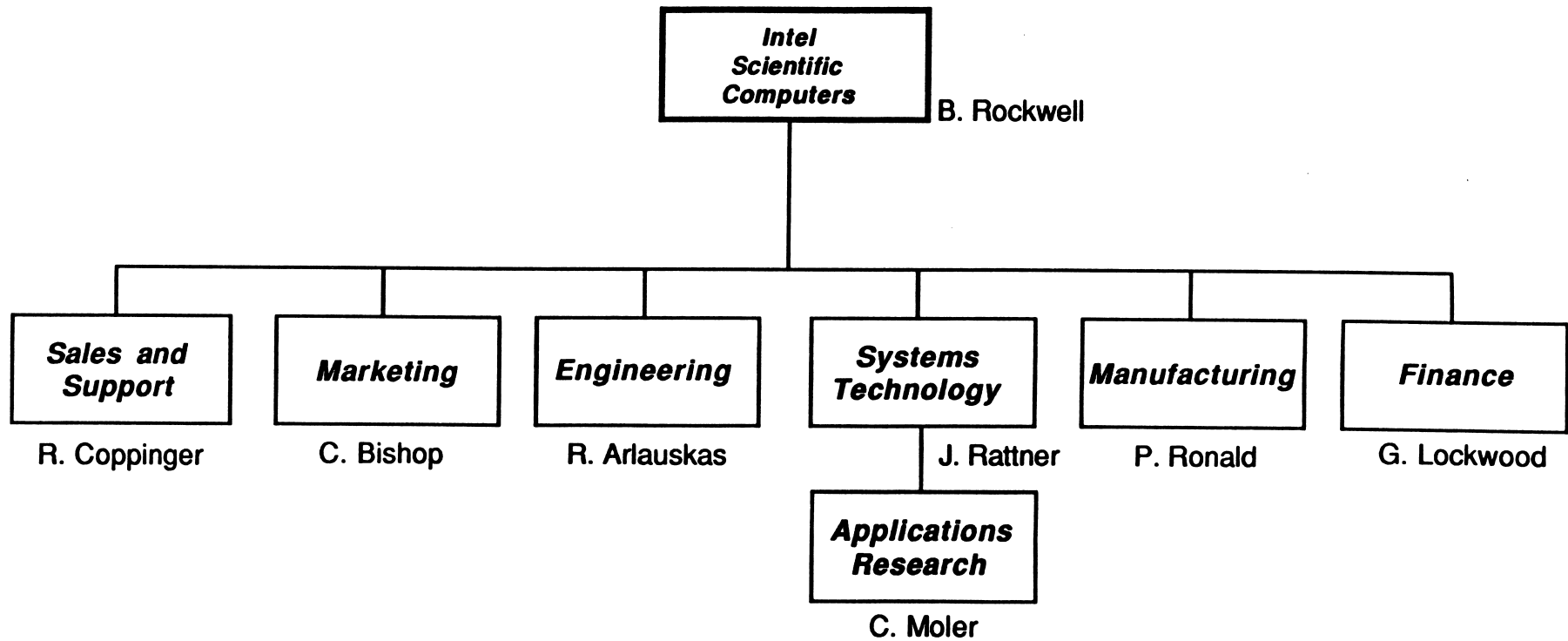
Intel Scientific Computers

...Intel Corporate relationship



Intel Scientific Computers

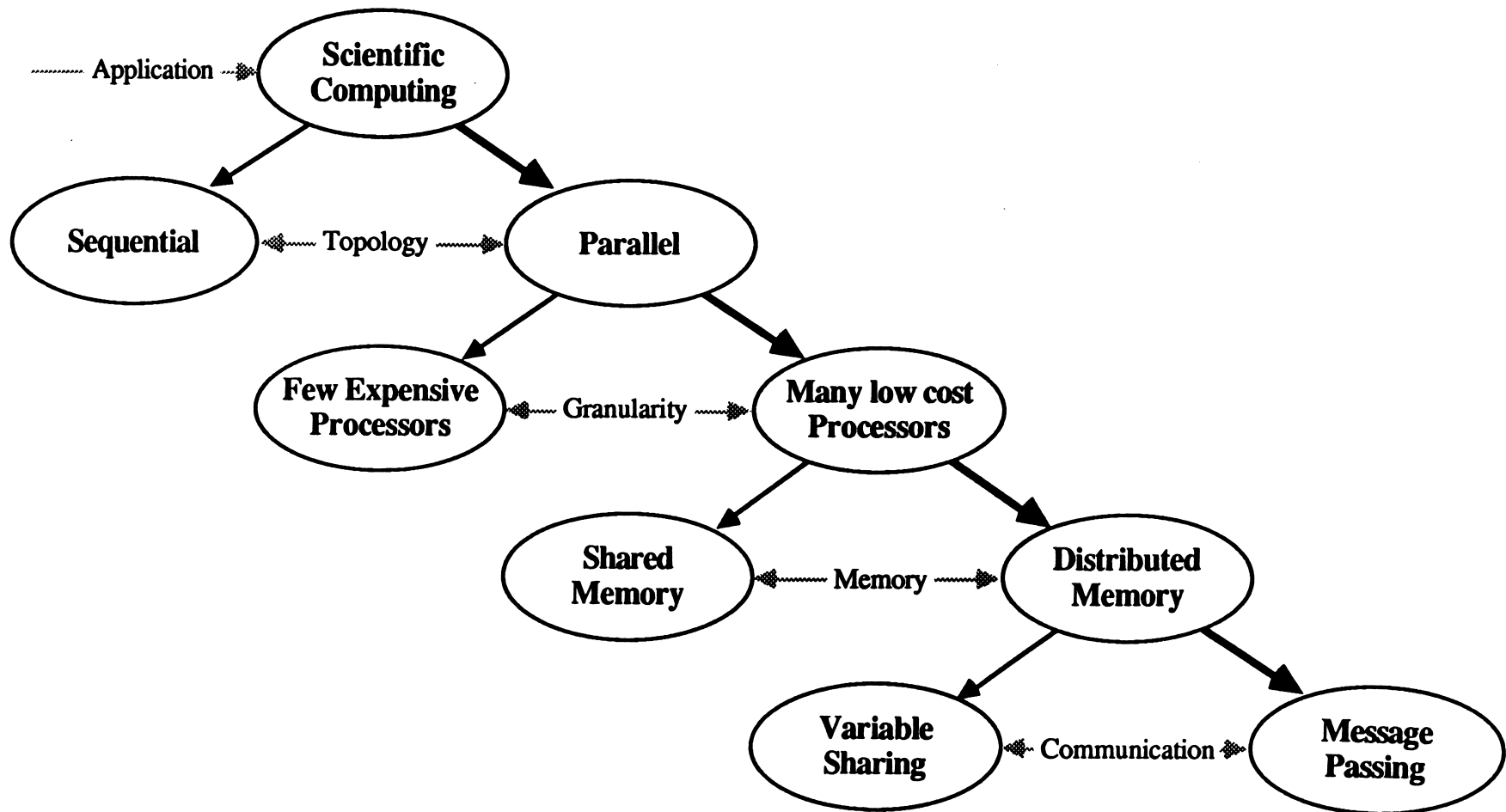
...management



Intel supported research in large-scale computaton

<i>Project</i>	<i>Institution</i>	<i>Architecture</i>
<i>Waterloop</i>	<i>Uni of Waterloo</i>	<i>8086/8087 -ring</i>
<i>VFPP</i>	<i>Columbia Uni</i>	<i>286/287 -2D mesh</i>
<i>MMCE</i>	<i>Carnegie Mellon Uni</i>	<i>8086/n x 8087 -bus</i>
<i>PRINGLE</i>	<i>Purdue/Uni of Washington</i>	<i>8051 -variable</i>
<i>DADO</i>	<i>Columbia Uni</i>	<i>8051 -tree</i>
<i>SPOCK</i>	<i>Georgia Tech</i>	<i>8086/8087 -variable</i>
<i>Cosmic Cube</i>	<i>Cal Tech</i>	<i>8086/8087 -hypercube</i>

Scientific Computing Architecture Alternatives



Intel Scientific Computers

...history

- April 1984*** ***iSC founded as an independent business unit***
- February 1985*** ***Announced the first commercial concurrent computer - iPSC***
- July 1985*** ***Shipped first system to Yale University***
- August 1985*** ***Announced our first enhancement: iPSC-MX memory board***
- Dec 1985*** ***Announced development agreement with Gold Hill Computers***
- April 14, 1986*** ***Announced the iPSC-VX enhancement:***
"Supercomputer performance at one-tenth the price"

Intel Scientific Computers

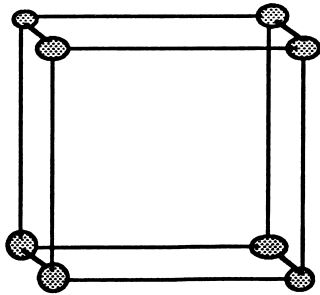
...history

- April 28, 1986** **Announced Concurrent Common LISP for the iPSC:
"First commercial LISP for a concurrent processor"**
- May 1986** **Installed CCLISP beta system at University of Southern Cal**
- August 1986** **Demonstrated experimental concurrent AI tools at AAAI '86**
- Sept 1986** **Shipped iPSC-VX beta system to Argonne National Labs**
- Oct 1986** **Shipped our 42th system**
-
- Nov/Dec ' 86** **Production shipments begin for CCLISP and iPSC-VX**

What is a hypercube?

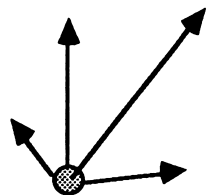
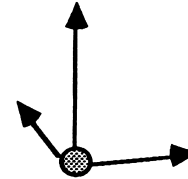
- 2^d processors, or nodes, each with local memory....
... "d" is the cube dimension
- Each node connected to "d" neighboring nodes
- Nodes pass messages to their neighbors, and/or to other nodes

Examples...



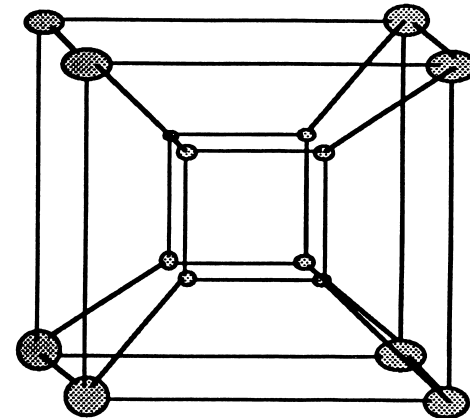
/d3 hypercube...

- each node connects to 3 neighbors
- $2^3 = 8$ nodes

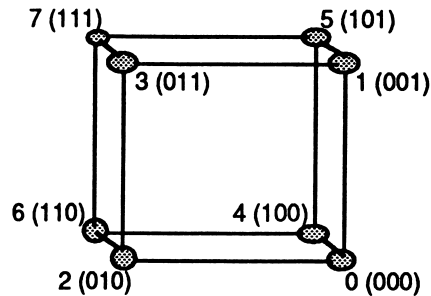


/d4 hypercube...

- each node connects to 4 neighbors
- $2^4 = 16$ nodes



Advantages of a hypercube?

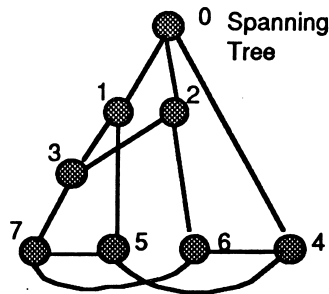


Elegant Topology-

- Nice relationship between popular numerical models and the system architecture

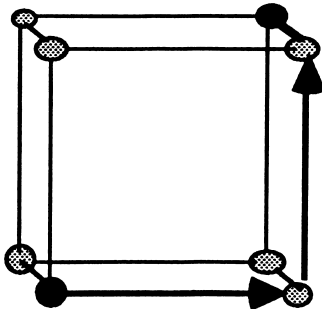
Flexible Topology

- Superset of current parallel topologies being applied
 - loop
 - mesh
 - toroid
 - ring
 - tree
- Nearest neighbor interactions dominate algorithms to maintain high observed efficiencies (0.8-0.9)

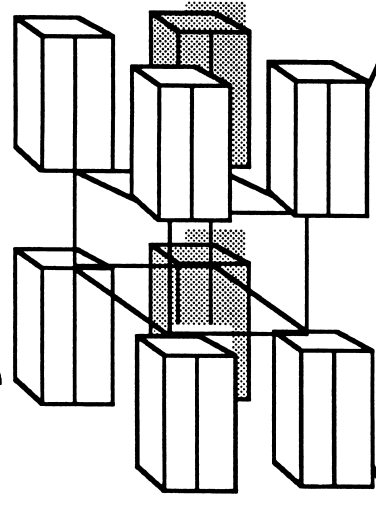


Efficient Topology- given "n" processors...

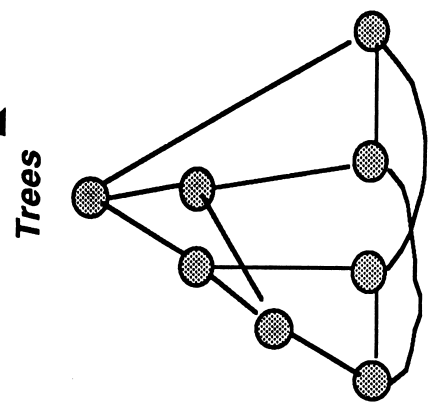
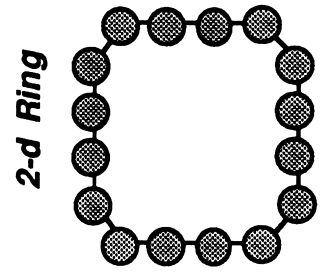
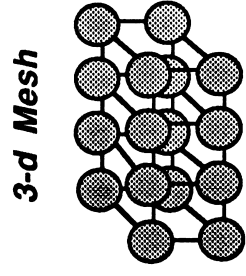
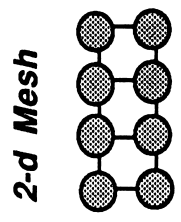
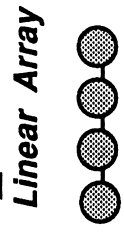
- Longest communications path is $\log n$... the cube dimension
- Average path is $1/2 \log n$
- Scalable- Aggregate bandwidth grows as $n \log n$



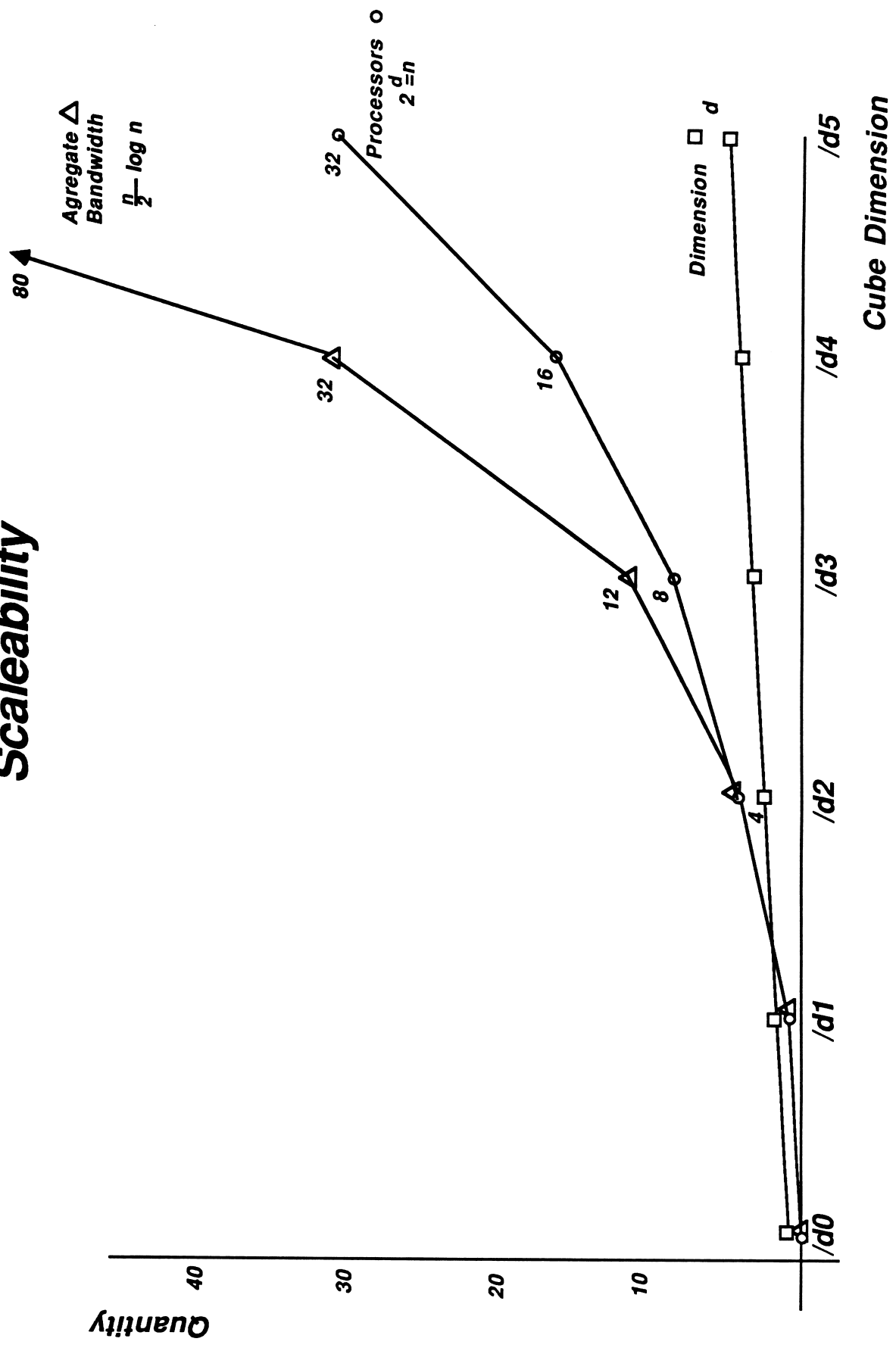
Maps Nicely To Other Topologies



Transformations Conserve
Nearest Neighbor Properties

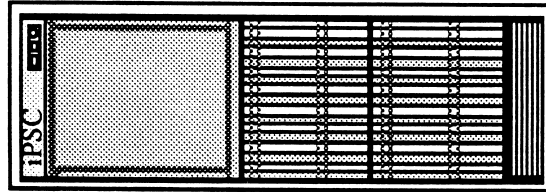


Scaleability



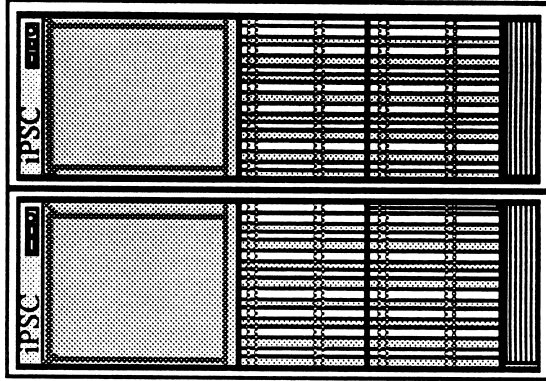
Intel's iPSC Hypercube Systems

iPSC/d5



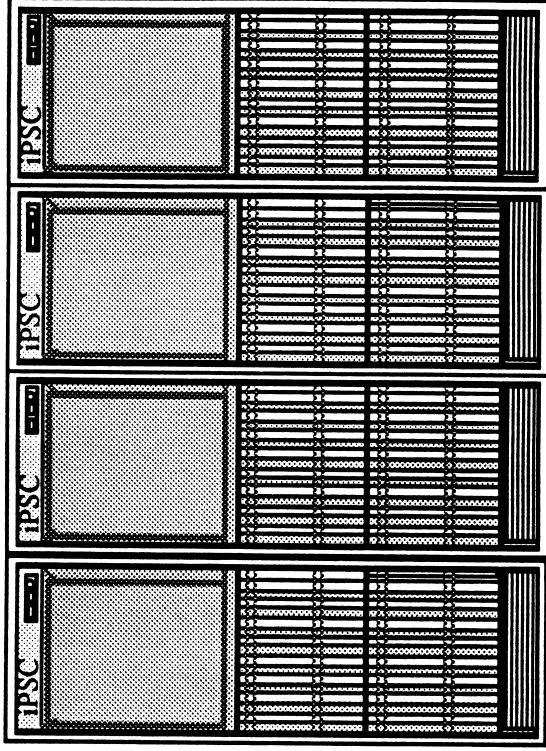
Single Unit
• 32 Card Positions

iPSC/d6



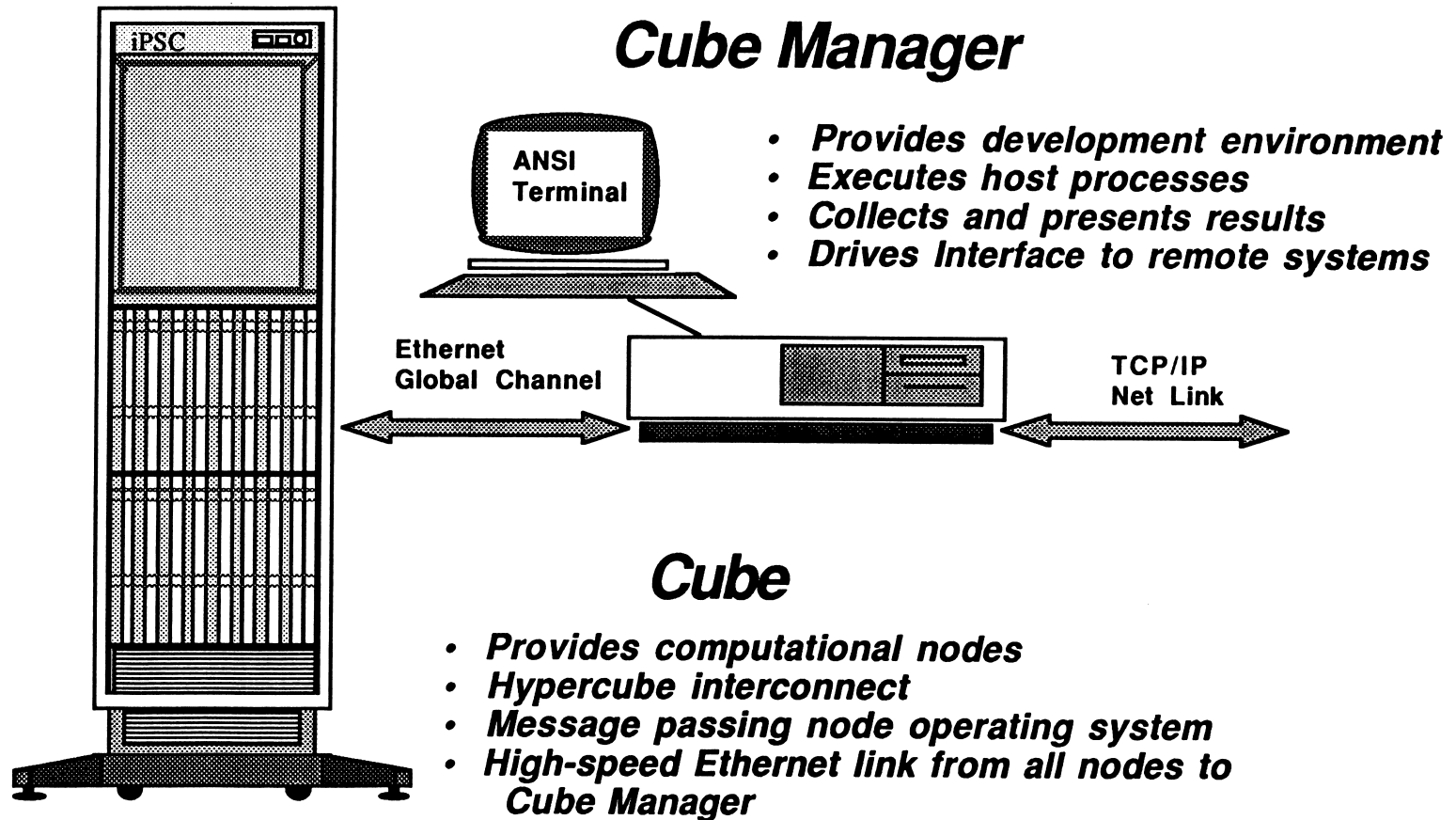
Double Unit
• 64 Card Positions

iPSC/d7

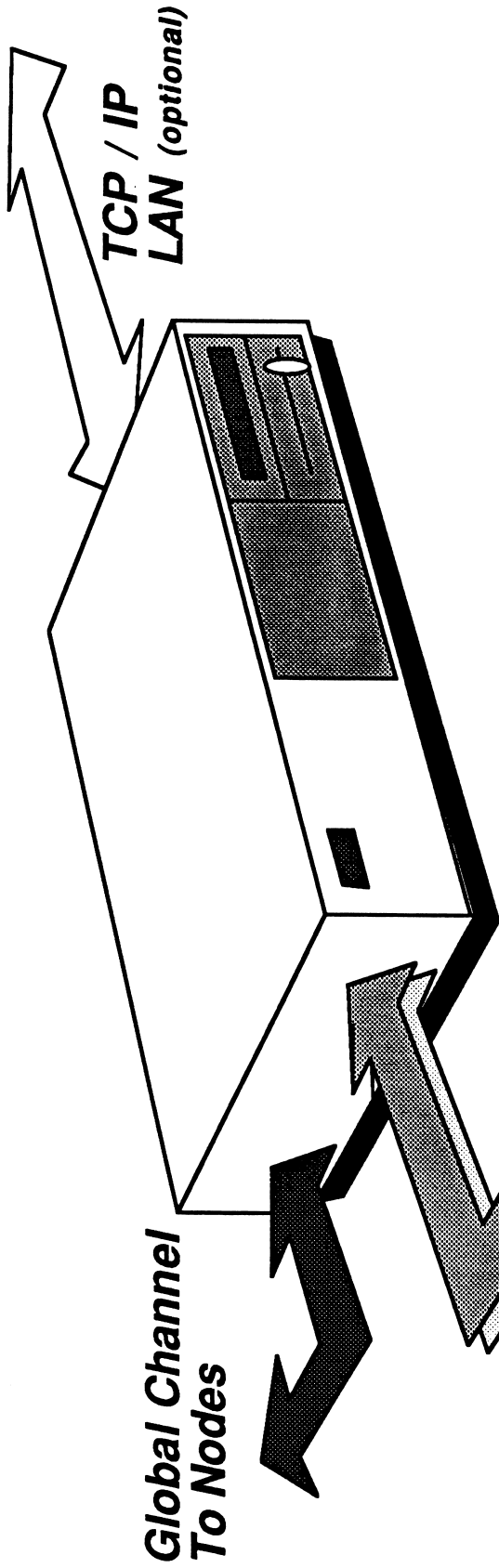


Quad Unit
• 128 Card Positions

iPSC Hardware Architecture



Cube Manager



**Global Channel
To Nodes**

**TCP / IP
LAN (optional)**

Features

- 140 MBytes Mass Storage
- 45 MByte Cartridge Tape
- 360 KByte Flexible Diskette
- High-speed 8 MHz '286' CPU
- 2 MBytes zero-wait-state RAM

ANSI Terminals

Expandable Up To 9

Options

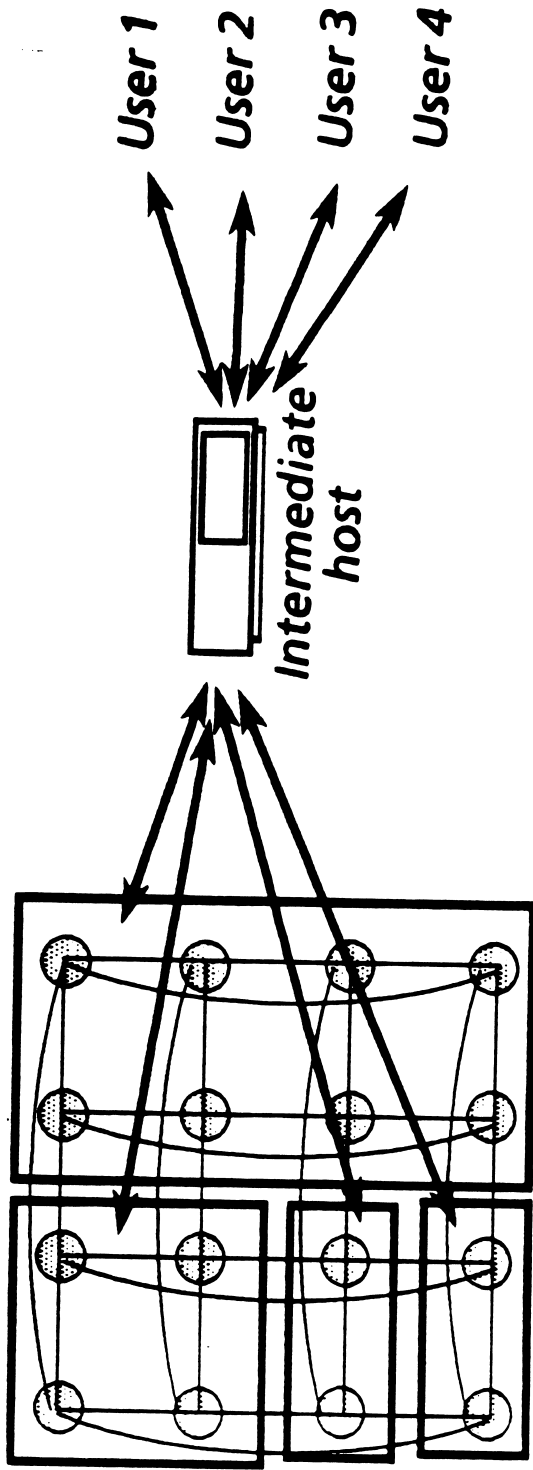
- Additional 2-4 MBytes RAM
- TCP /IP LAN
- Additional 8 Serial I/O Channels

• • NOTICE • •

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Cube Sharing

(available 1Q '87)

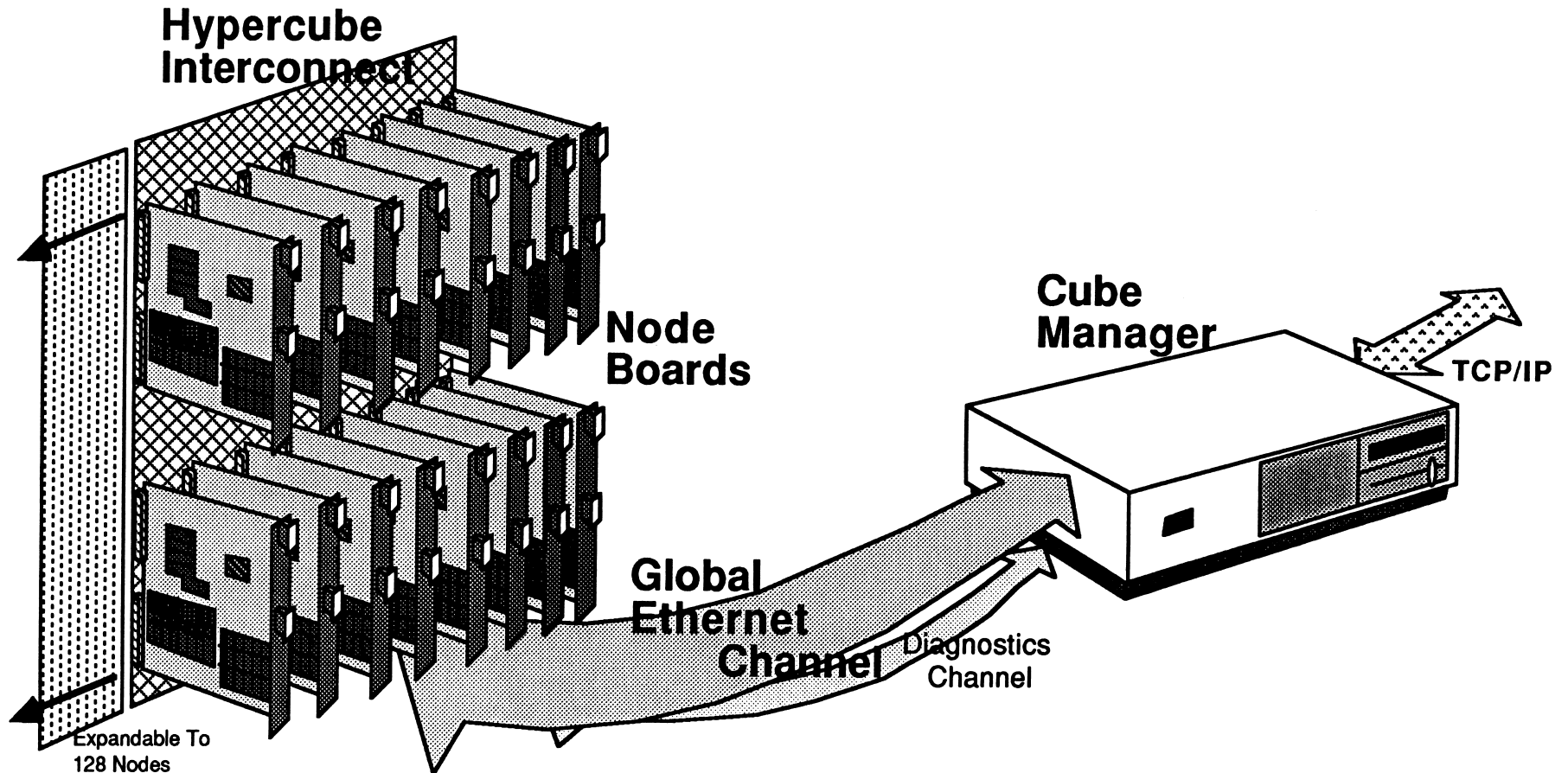


Hypercube nodes

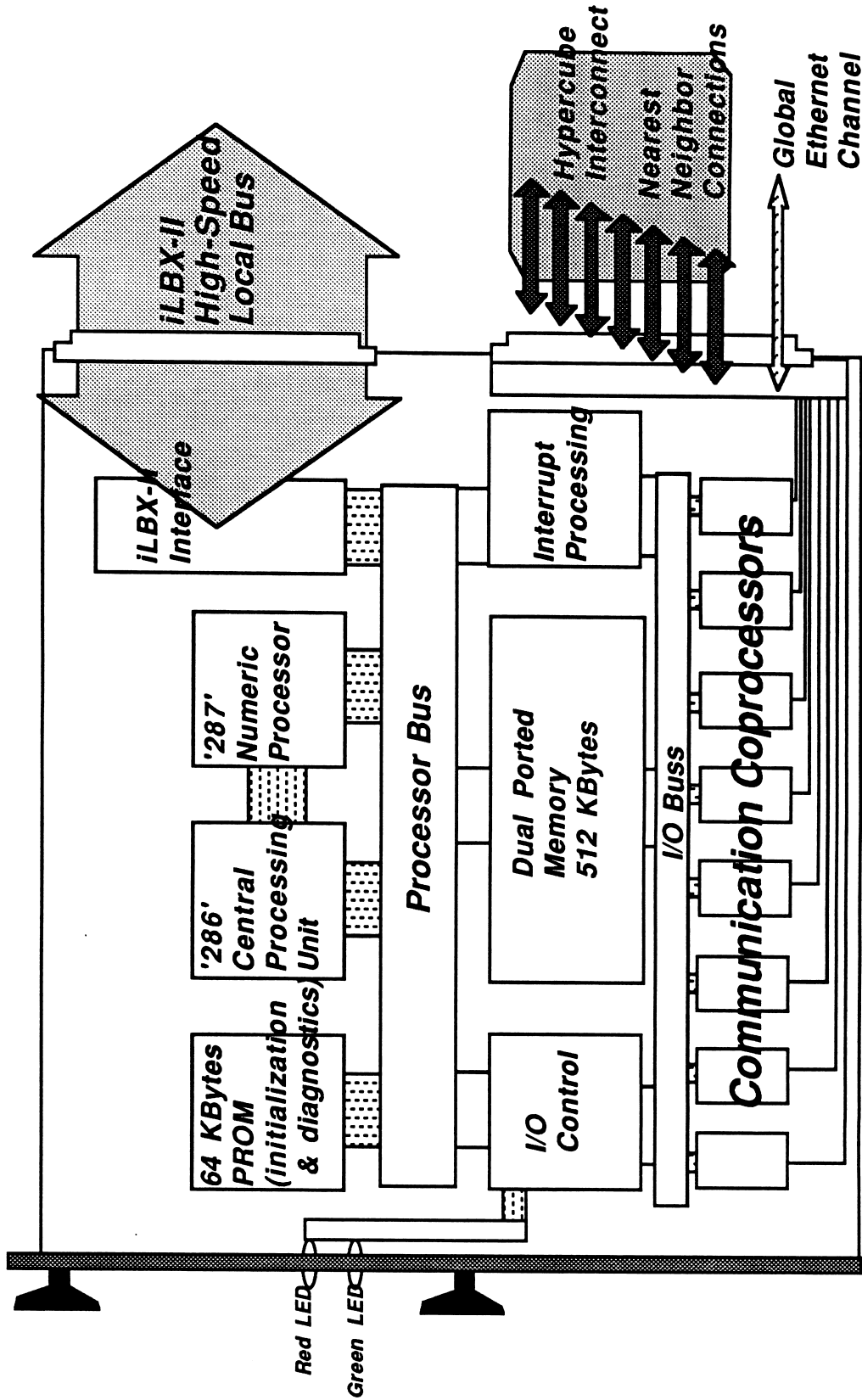
Multuser Operation

- Subcubes served to each requesting user
- Intermediate host maps physical nodes to logical subcube requests

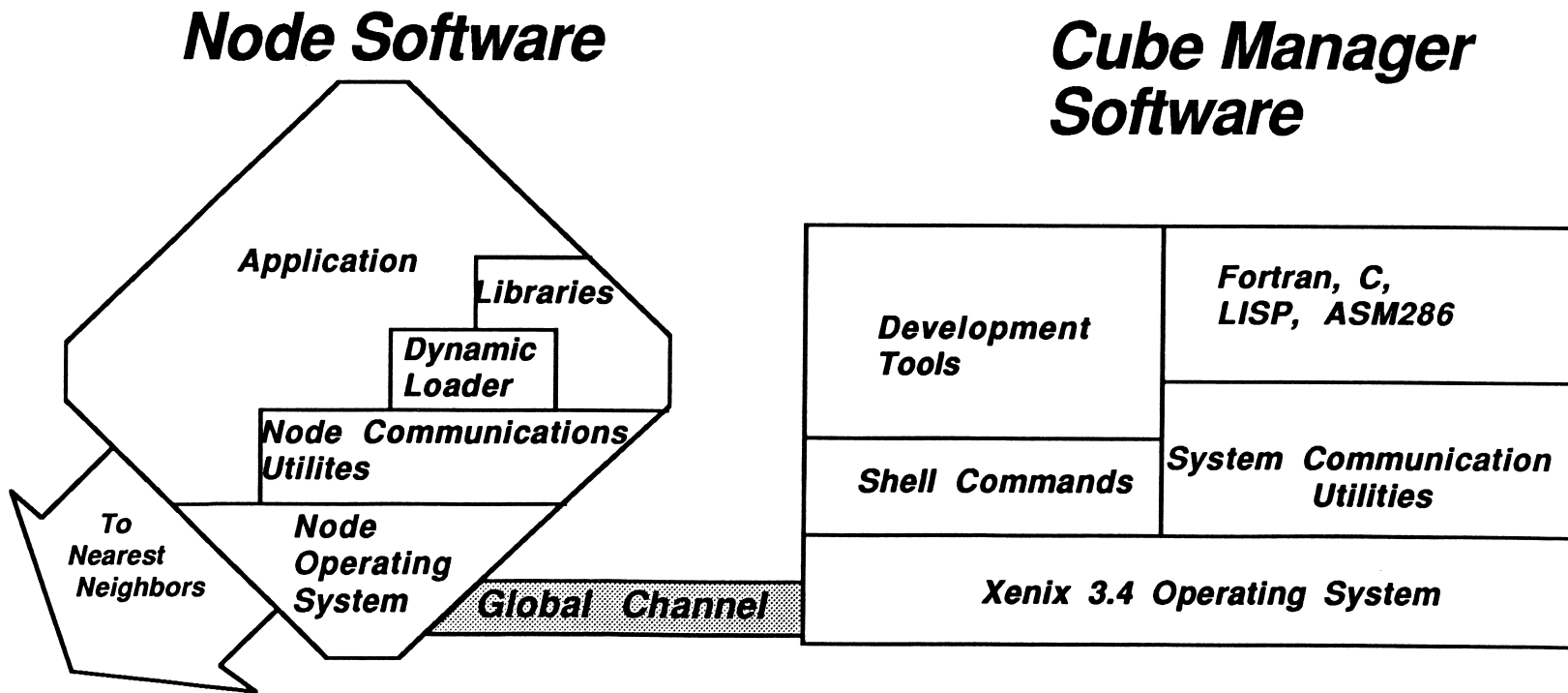
Communication Channels



Node Architecture



System Software Architecture



Languages & Tools

Languages-

- FORTRAN
- 'C'
- Macro Assembler (ASM286)
- Goldhill Concurrent Common Lisp

Tools-

- Simulator
- Dynamic Loader
- Debugger

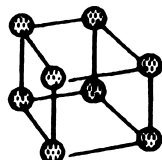
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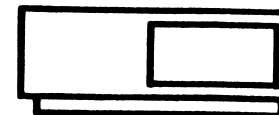
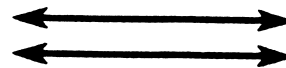
Concurrent Debugger

(beta-test version available Nov. 86)

Sequential Capabilities	Concurrent Capabilities
<ul style="list-style-type: none">● <i>Source-level debug for FTN77, C</i>● <i>Data access/update</i>● <i>Breakpoint, trace</i>● <i>Execution monitoring</i>	<ul style="list-style-type: none">● <i>Process monitoring & control</i>● <i>Communications monitoring & control</i>● <i>Node status</i>● <i>Message status</i>



Executable at each node



Executable from host

Utilities Callable From FORTRAN , 'C', LISP

Cube Manager Utilities

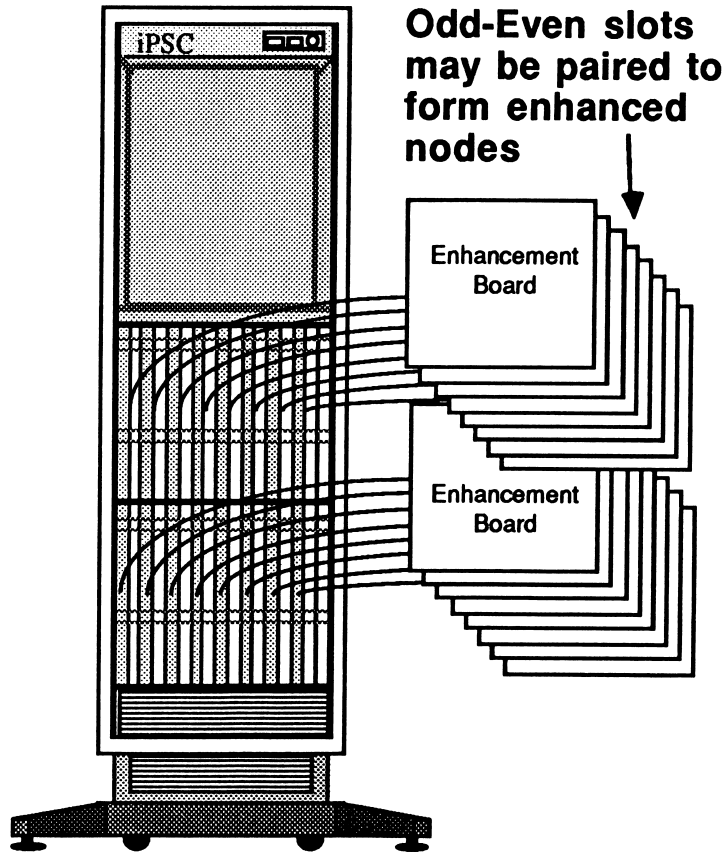
- **load-** load & start program
- **lkill-** kills selected process(es)
- **lwait-** waits on process(es)
- **sendmsg/recvmsg-** send or receive message
- *mypid- determine process identifier*
- *copen/cclose- open or close a comm channel from process to another process*
- *cubedim- determine cube dimension*

Utilities Callable From FORTRAN , 'C', LISP

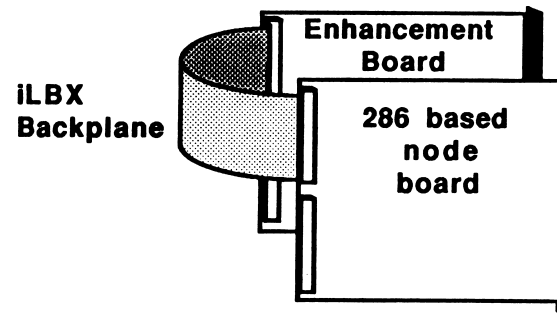
Node Utilities

- ***send/recv-*** ***send or receive message from one process to another***
- ***copen/cclose-*** ***open or close a comm channel***
- ***cubedim-*** ***determine dimension of cube***
- ***syslog-*** ***send message to system log***
- ***mynode-*** ***determine node identifier***
- ***clock-*** ***get clock time in milliseconds***
- ***flick-*** ***defer process execution***
- ***probe-*** ***determine if message type is available***
- ***status-*** ***determine if message has been sent or received***
- ***handler-*** ***invokes user-written exception handler***

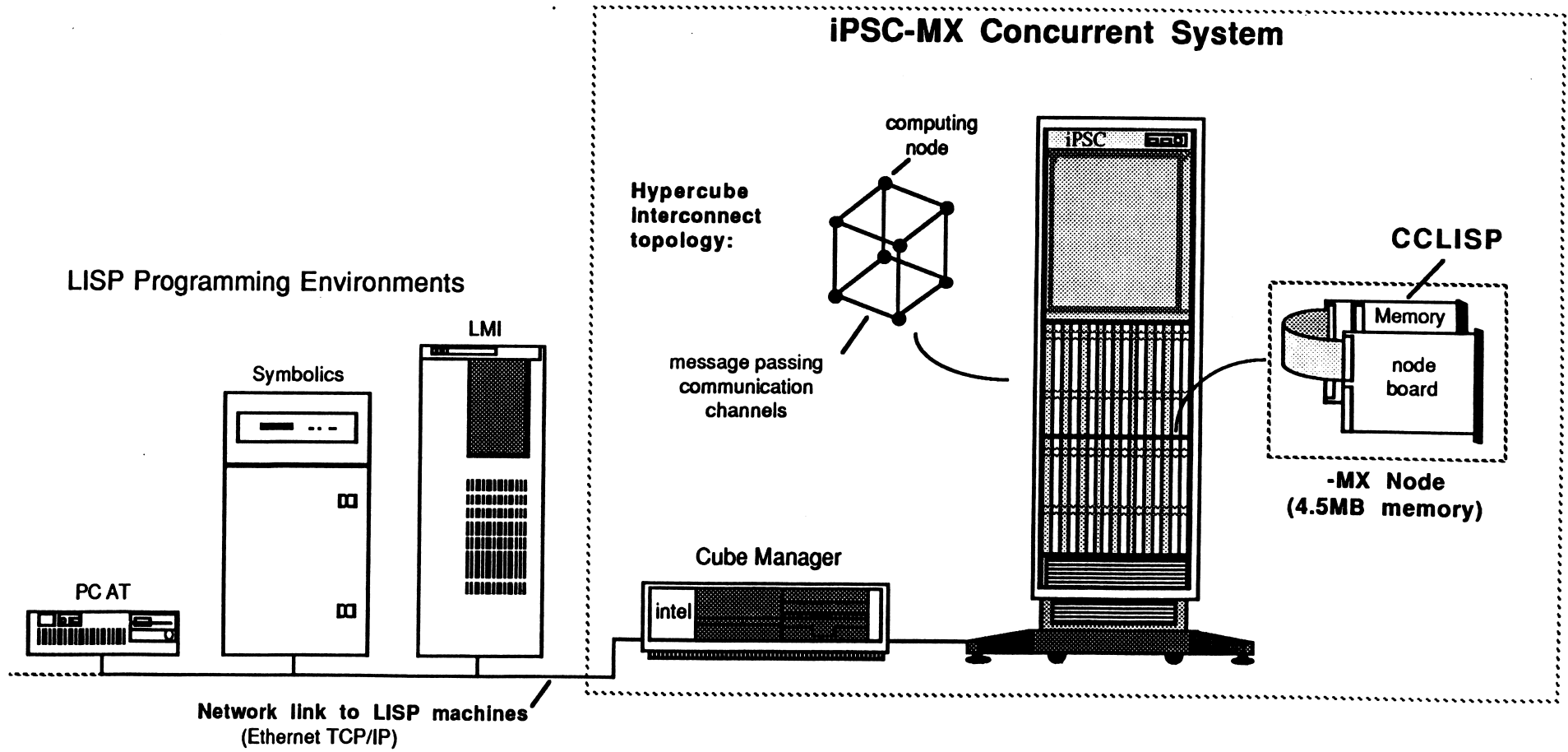
Open To Enhancements From Intel, From Independent Efforts



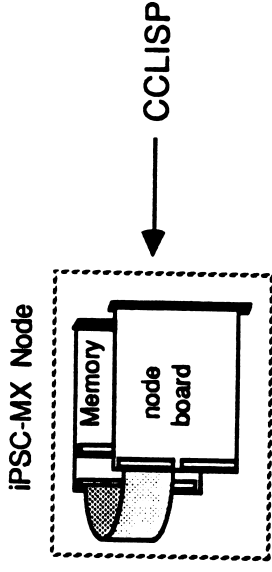
- **Available As /d4MX, /d5MX, /d6MX Large Memory Systems**
- **Available As /d4VX, /d5VX, /d6VX Vector Systems**
- **Or, independently developed to iLBX-II standard interface**



iPSC/CCLISP Product Overview

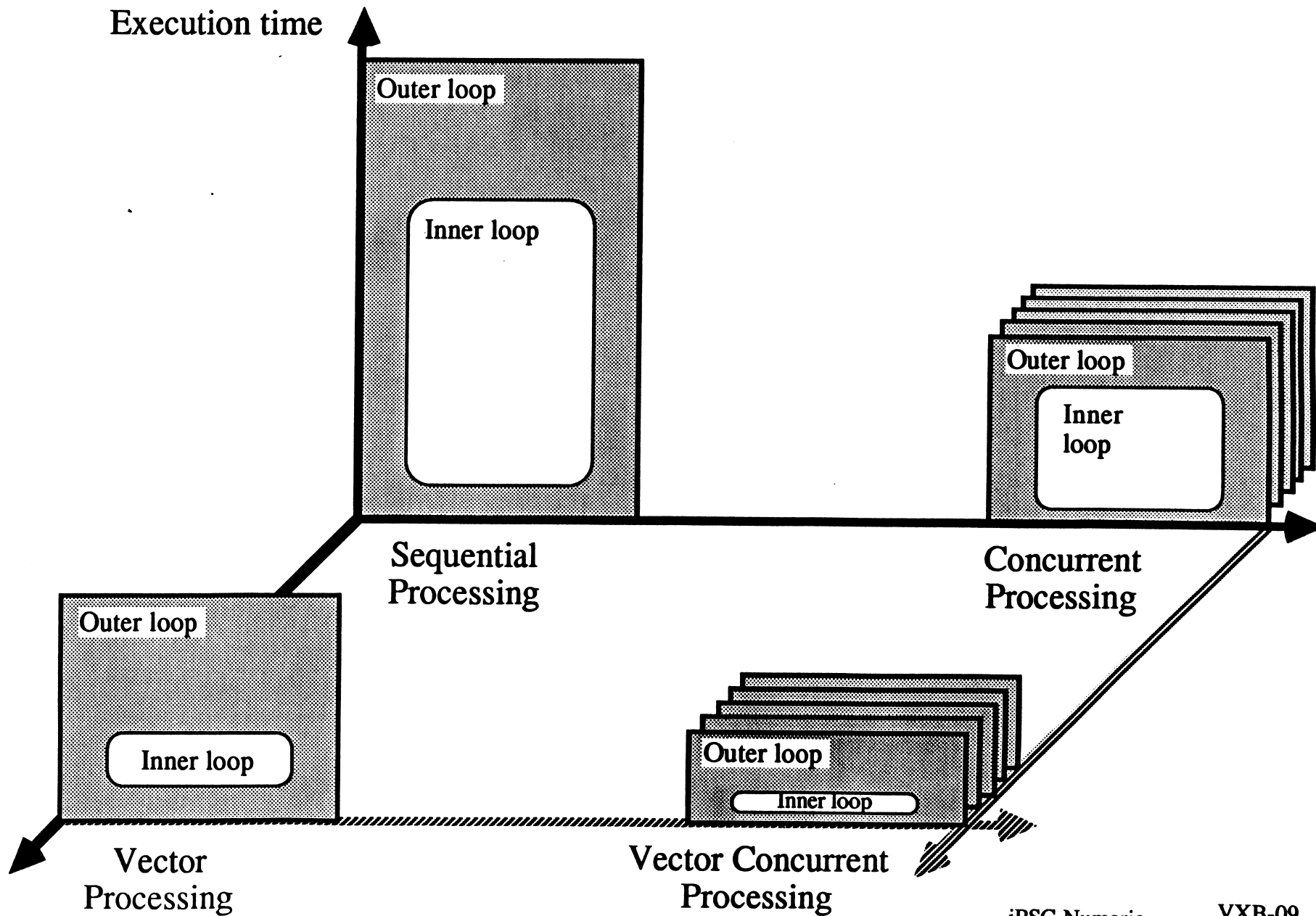


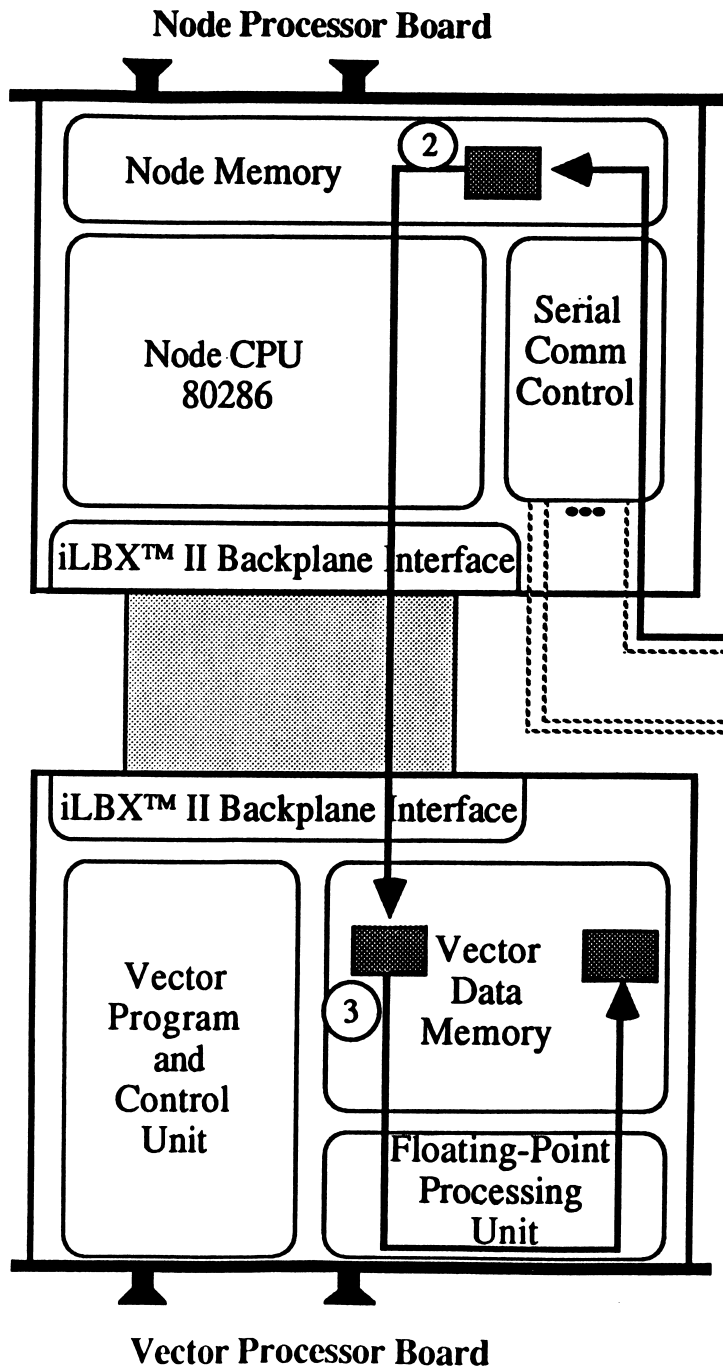
CCLISP on each -MX node



- ***Industrial Quality***
 - *Optimized for the 80286*
 - *Compiler as well as interpreter (8x performance)*
 - *Lexical scoping instead of dynamic scoping*
 - *Large memory (15 MB) addressability*
 - *80287 math coprocessor fully supported*
- ***Based on Gold Hill's GCLISP 286 Developer***
- ***CCLISP is a subset of Common LISP, extended for concurrency***
- ***CCLISP contains all of the features necessary for the demands of commercial customers-***
 - Lexical scoping* • *Integers and floating-point numbers* • *characters and strings* • *Symbols and packages* • *Streams and pathnames* • *Vectors and one-dimensional arrays*
- ***Remote eval***

Vector Concurrent Computing

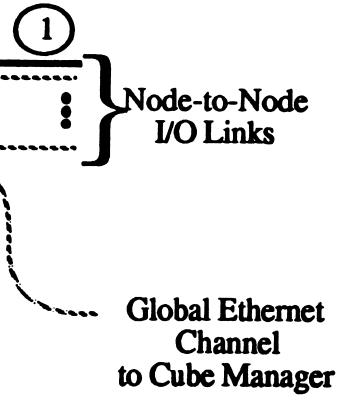




iPSC-VX:

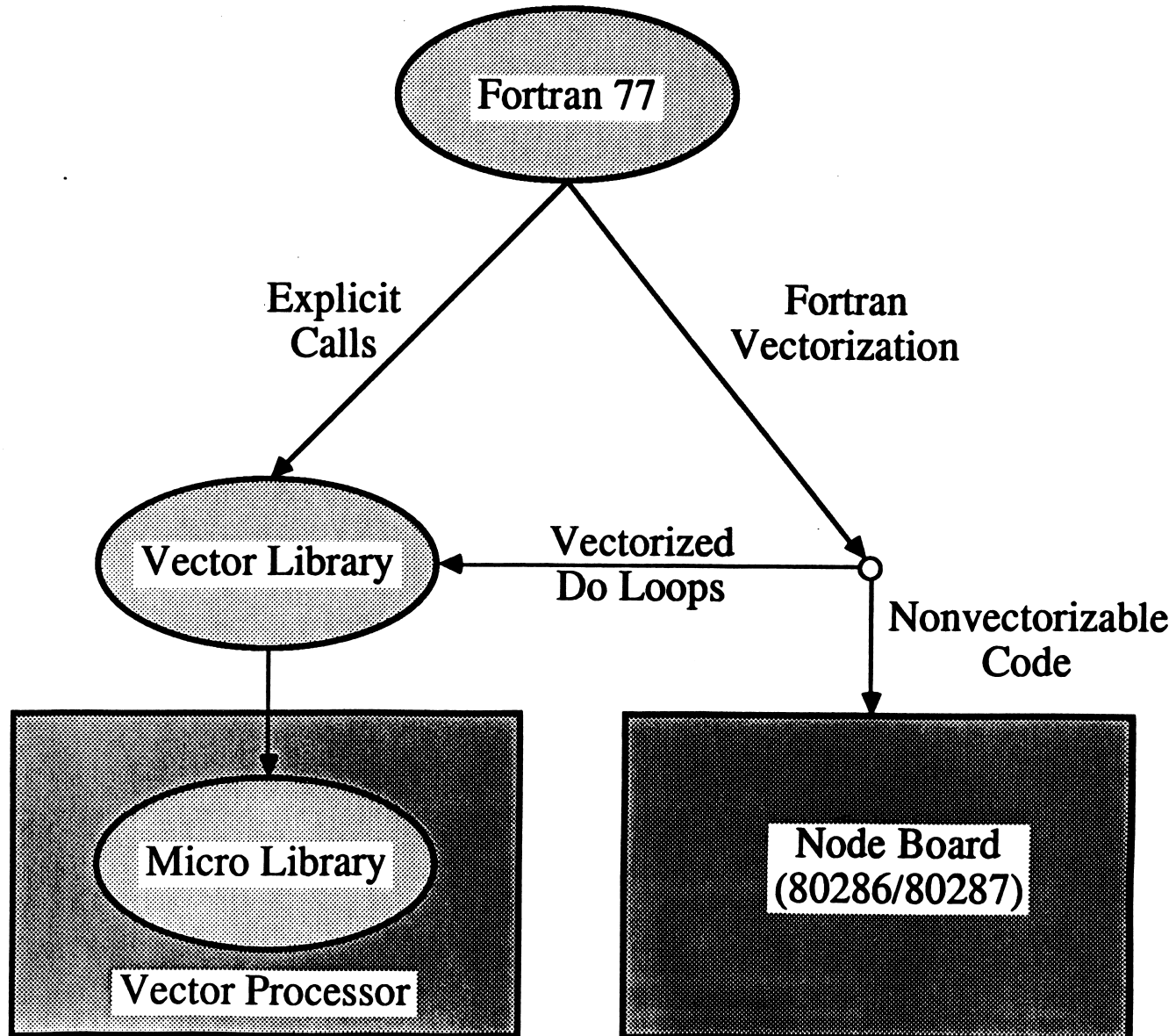
Message based communication

- ① Message is received and deposited in communications buffer
- ② Node OS matches message in buffer with RECV executed by node process and OS moves data into process work space



- ③ Node process initiates execution of VP task to process data.

Harnessing the Vector Processor



A Parallel Example

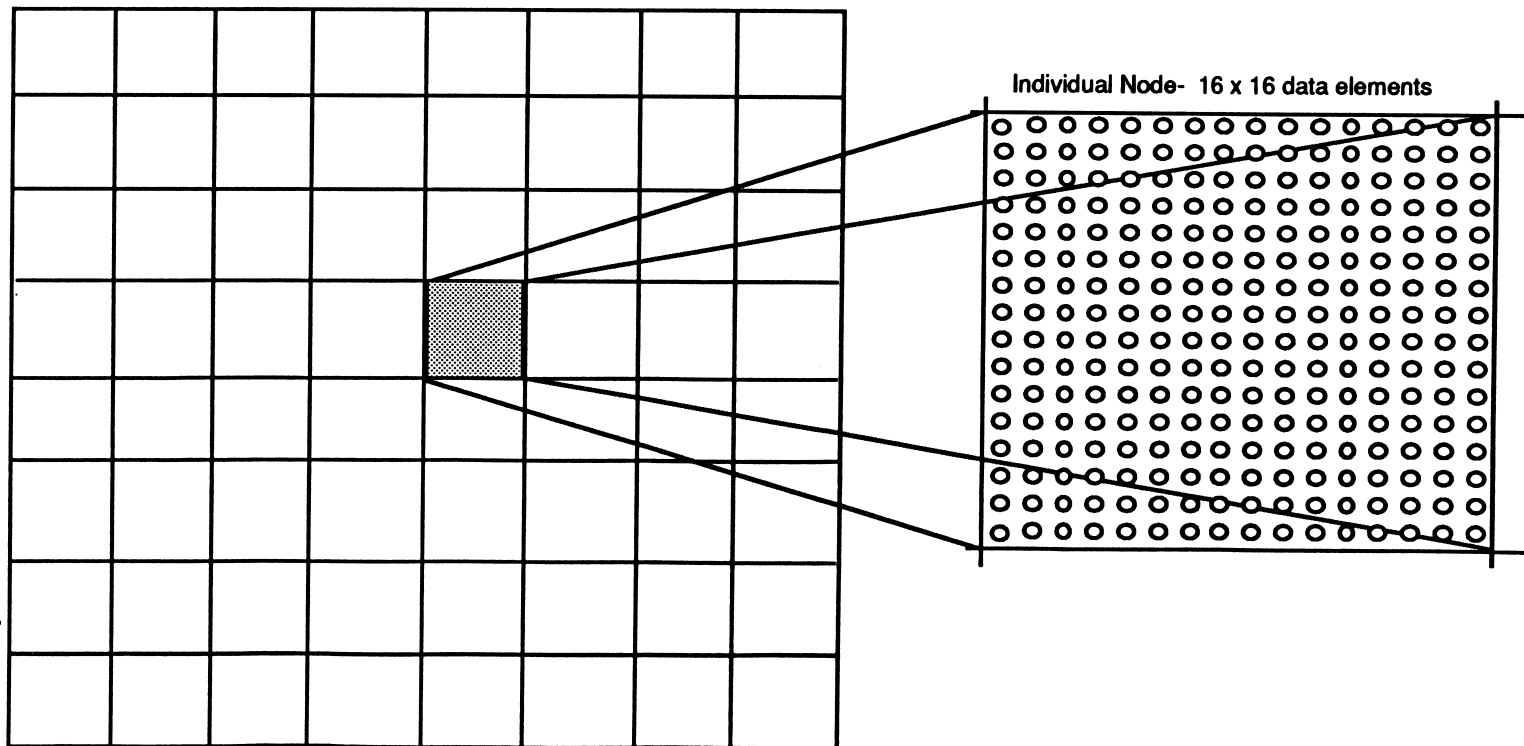
Relaxation Problem- Laplace Equation, 2nd order differential

$$\nabla^2 \phi = 0$$

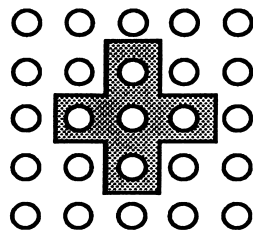
$$\text{or- } \frac{\partial^2 x}{\partial t^2} + \frac{\partial^2 y}{\partial t^2} = 0$$

Ex: Temperature Across A Black Body

Problem Space: 16K Data Elements Distributed Over 64 Node System



New Element Values Are Computed By Averaging 4 Nearest Neighbors



Pictorial View

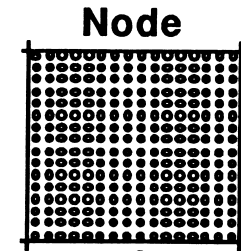
||

a11	a12	a13	a14	a15
a21	a22	a23	a24	a25
a31	a32	a33	a34	a35
a41	a42	a43	a44	a45
a51	a52	a53	a54	a55

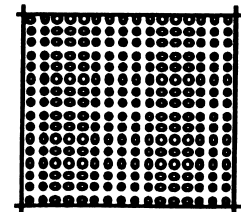
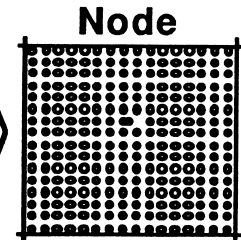
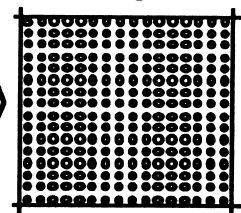
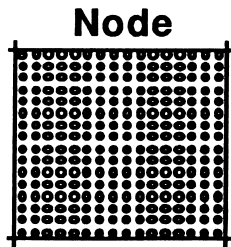
Matrix View

||

$a_{33}' = (a_{23} + a_{32} + a_{34} + a_{43})/4$ Arithmetic View



- Central elements of matrix computed immediately
- Edge elements require values from neighboring processors



Node

Applications & Algorithms

Geophysics

- Oil reservoir modeling
- Mantle Dynamics
- 3-D Seismic
- Granular Motion

Image Processing

- Graphics
- Image Synthesis
- Animation
- Image Enhancement

Computer Science

- Algorithms
- Artificial Intelligence
- Languages
- Operating Systems

Chemistry

- Molecular Dynamics
- Molecular Chemistry
- Quantum Chemistry
- Quantum Mechanics
- Statistical Mechanics

Computational Algorithms

- Finite Element Modeling
- Finite Difference Equations
- FFT & Filter Techniques
- Sparse Matrix Equations
- Partial Differential Equations
- Ordinary Differential
- Monte Carlo Simulations
- Relaxation Techniques
- Ray Tracing

Electrical Engineering

- Linear Circuit Simulation
- Rules Checking
- Logic Simulation

Physics

- Quantum Field Theory
- Fluid Mechanics
- Astrophysics
- High Energy Physics
- Meteorology

Mechanical Engineering

- Structural Analysis
- Fluid Dynamics

Biochemistry

- Genetic Engineering
- Pharmaceutical Research

Aerospace Engineering

- Aerodynamics
- Structural Mechanics

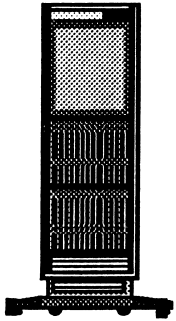
Applications Development Activity

Application	Name	Developer(s)
Fluid Dynamics	Lax-Wendroff	UCSB
Peptide Energy	ECEPP83	Oregon Grad Ctr.
Molecular Modeling	Gaussian 86	Hypercube, Inc.
Image Synthesis	Genisys® (version)	Visual/Kobra Graphics
Oil Reservoir Modelling	VIP	J.S. Nolen, Associates
Semiconductor Modeling	Pices	Stanford Univ.
Structural Analysis	NICE-SPAR	Lockheed/NASA
Heat Transfer/Fluid Dynamics	Nekton	Nektonics, Inc.
Circuit Simulation	n.a	Several
Place and Route	Timberwolf.	CMU

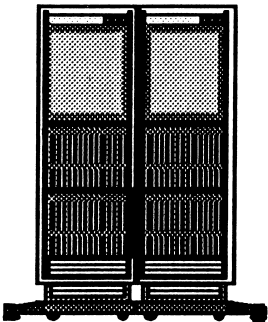
Tool Development Activity

Application	Name	Developer
Dense Matrix Solver	LINPACK	iSC App's Research
Eigenvalues/Eigenvectors	EISPACK	iSC App's Research
Sparse Matrix Solver	SPARSPAK	Oak Ridge Nat. Lab
Extended Matrix-Vector	Ext. BLAS	Argonne Nat. Lab
Differential Eq. Solver	FISHPAK	U. Colorado Denver
Scientific Utilities	NAG	NAG
FORTTRAN Parallelizer	n.a.	Rice University
Simple Operating System	CrOS	Caltech Physics
Distributed Ada	Ada	U. Michigan

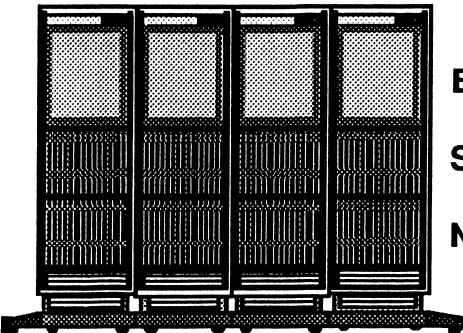
The iPSC System Family



	<u>Name</u>	<u>Nodes</u>	<u>Memory</u>	<u>MFLOPS</u>	<u>Price</u>
Base System	iPSC/d5	32	16 MBytes	2	\$155K
Symbolic System	iPSC/d4-MX	16	72 MBytes	1	\$176K
Numeric System	iPSC/d4-VX	16	24 MBytes	106	\$250K



Base System	iPSC/d6	64	32 MBytes	4	\$280K
Symbolic System	iPSC/d5-MX	32	144 MBytes	2	\$306K
Numeric System	iPSC/d5-VX	32	48 MBytes	212	\$450K



Base System	iPSC/d7	128	64 MBytes	8	\$525K
Symbolic System	iPSC/d6-MX	64	288 MBytes	4	\$555K
Numeric System	iPSC/d6-VX	64	96 MBytes	424	\$850K

Intel iPSC™ System

Summary Of Intel Business Position

- **Market Leadership**
- **Corporate capability**
- **Long-term commitment**

Intel iPSC™ System

The iPSC System Today

- **1½ years applications leadership**
- **Largest installed base of users, systems**
- **New vector-concurrent computing enters era of affordable supercomputers**
- **Key system technology developments underway**

Large-scale Concurrent Market Perspective

- **Market size to exceed 100 this year**
 - ~ 50% universities
 - ~ 40% government related
 - ~ 10% industrial

... iPSC installations mix
- **Broad based parallel technology development...**
 - concurrent operating systems
 - concurrent languages & tools
 - concurrent algorithms
 - modeling and simulation
 - ISV application packages
- **Market installations expected to more than double in '87**
 - ... greatly increased activity in:
 - > defense contractors
 - > private industry
 - ... particular interest in numeric & symbolic together
- **Primary market motivation -> parallel computation is the future!**

Intel Strengths

- **Over 40 iPSC system installations worldwide**
 - **1st commercial vendor to market**
 - **Installations worldwide**
- **14 months of field experience in the research community**
 - **130+ users in leading research institutions worldwide**
 - **Maturing system software**
 - > **improvements in reliability, performance, and programmer productivity**
- **Reliable hardware/stable software and a proven concurrent architecture**
- **Numeric and symbolic capabilities in same machine**
- **Wide acceptance of the iPSC by government funding agencies**
- **Access to state-of-the-art concurrent expertise**
 - **Close ties to the concurrent research community**
 - **Inhouse applications research group**
 - **iPSC users group**
- **Intel corporate commitment to parallel computers**
 - **Strategic business for Intel**
 - **Intel VLSI technology is critical to success**
 - **iSC market leadership**